Amendments to the Claim:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1, 3, 12, 15-28; add 29-36, change the dependence of claims 2, 7-11, and 13, and add new claims 29-36, all without prejudice. The other pending claims are all as previously submitted.

Listing of the Claim:

(Claim 1 has been cancelled.)

2.(Currently Amended) The memory system circuit of claim 29 ~~1~~, further comprising:

a bus connected to transfer data between the controller and the data storage sections whereby data is transferable to the second data storage section while data is being programmed into the first data storage section.

(Claim 3 has been cancelled)

4.(Original) The memory system circuit of claim 2, wherein each of the data storage sections comprises a data register wherein data transferred from the controller is stored.

5.(Original) The memory system circuit of claim 4, wherein each of the data storage sections further comprises an array of non-volatile storage units into which data stored in the data register is programmed.

6.(Original) The memory system circuit of claim 4, wherein each of the data storage sections further comprises a RAM memory section connected to store a copy of the data transferred into the data register.

7.(Currently Amended) The memory system circuit of claim 29~~-1~~, wherein the controller, the first data storage section and the second data storage section are on separate chips.

8.(Currently Amended) The memory system circuit of claim 29~~-1~~, wherein the first data storage section and the second data storage section are on a single chip.

9.(Currently Amended) The memory system circuit of claim 29~~-1~~, wherein the controller, the first data storage section and the second data storage section are on a single chip.

10.(Currently Amended) The memory system circuit of claim 29~~-1~~, wherein the controller, the first data storage section and the second data storage section are part of a single card structure removably attachable to a host.

11.(Currently Amended) The memory system circuit of claim 29~~-1~~, wherein the controller is embedded in a host and wherein the first data storage section and the second data storage section are part of a single card structure removably attachable to the host.

(Claim 12 has been cancelled.)

13.(Currently Amended) The method of claim 33~~-12~~, further comprising:

subsequent to the transferring the second set of data, programming the second set of data into the second storage section, wherein programming the second set of data starts during the programming the first set of data.

14.(Original) The method of claim 13, further comprising:

subsequent to the programming the first set of data, performing an erase operation in the first storage section, wherein the erase operation starts during the programming the second set of data.

(Claims 15-28 have been cancelled.)

29.(New) A memory system circuit, comprising:

a controller comprising a first and a second data buffer connectable to receive host data from external to the memory system; and

a memory comprising a plurality of independently controllable non-volatile data storage sections connectable to the controller to receive data,

wherein, concurrently with the programming of data into a first of the data storage sections, data is transferable from either of said data buffers to a second of the data storage sections, and

wherein, concurrently with the transferring of data from one of said data buffers to the second of the data storage sections, host data from external to the memory system can be received into the other of said data buffers.

30.(New) The system circuit of claim 29, wherein subsequent to the transfer of a data set from one of the buffers to one of the data storage sections, during the programming of said data set into said one of the data storage sections, a copy of said data set is maintained in said one of the buffers until said programming of said data set into said one of the data storage sections is completed.

31.(New) The system circuit of claim 29, wherein subsequent to the transfer of a first data set from one of the buffers to one of the data storage sections, during the programming of the first data set into said one of the data storage sections, a second data set from external to the memory system is received in said one of the buffers prior to the completion of said programming of said data set into said one of the data storage sections.

32.(New) The system circuit of claim 29, wherein said programming of data into a first of the data storage sections comprises the concurrent programming of multiple sectors of data.

33.(New) A method of operating a non-volatile memory system comprising a controller including a plurality of data buffers and a memory including a plurality of independently controllable non-volatile data storage sections, the method comprising:

transferring a first set of data from an external source to a first of the data buffers;

transferring said first set of data from the first data buffer to a first of the data storage sections;

programming the first set of data into the first storage section;

transferring a second set of data from the external source to a second of the data buffers concurrently with said transferring said first set of data from the first data buffer to a first of the data storage sections; and

transferring said second set of data from the second data buffer to a second of the data storage sections concurrently with said programming the first set of data into the first storage section.

34.(New) The method of claim 33, wherein subsequent to said transferring said first set of data from the first data buffer to a first of the data storage sections, a copy of said first data set is maintained in said first buffers until said programming the first set of data into the first storage section is completed.

35.(New) The method of claim 33, further comprising:

subsequent to said transferring said first set of data from the first data buffer to a first of the data storage sections, transferring a third set from the external source to the first data buffers prior to the completion of said programming the first set of data into the first storage section.

36.(New) The method of claim 33, wherein said data sets comprise multiple sectors of data and wherein said programming comprises the concurrent programming of multiple sectors of data.